Estd: 1998

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC – AUTONOMOUS INSTITUTION)

(Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi)
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Schedule -M. Tech (VLSI Design & Embedded Systems) II Year I Semester (R24) Mid- Term Test -I October -2025

Academic Year – 2025-2026 (For 2024 Admitted batch)

Skill Enhancement Course

Branch	Date &Day	Session &Time	Roll Nos	Course Name /Code	Lab No
M.Tech	16.10.2025 (Thursday)	FN: 11:10 AM-01:10 PM	24691D6901-24691D6915	QNX Embedded Real Time Operating System (24VESP601)	EB-103

P.Kanthan

PRINCIPAL
Principal
Madanapalle Institute of
Technology & Science
MADANAPALLE